FULLY MONOLITHIC INTEGRATED EVEN HARMONIC QUADRATURE RING MIXER WITH AN ACTIVE MATCHED 90 DEGREE POWER DIVIDER FOR DIRECT CONVERSION RECEIVERS

Kenji KAWAKAMI, Ken'ichi TAJIMA, Mitsuhiro SHIMOZAWA,
Kenji ITOH, Nobuyuki KASAI and Akio IIDA
Information Technology R&D Center, Mitsubishi Electric Corp.
5-1-1 Ofuna, Kamakura-city, Kanagawa 247,JAPAN
TEL: 0467-41-2549, FAX : 0467-41-2519, E-mail :kawaken@micro4.isl.melco.co.jp

Abstract

This paper proposes a novel circuit configuration of an even harmonic quadrature mixer for direct conversion receivers. The proposed configuration employs a ring mixer concept for wide-band reception and active matching circuits for a full integration on a small sized GaAs chip. Highly stable quadrature detecting characteristics over LO power variation can be achieved by the proposed active matched 90 degree power divider. A developed 2GHz MMIC achieves an extremely small chip size of 1.3mm ~1.85mm, and good quadrature detecting characteristics with amplitude error within 0.5dB and phase error within 5 degrees from 1.7GHz to 2.3GHz.

Introduction

Direct conversion receivers, that convert RF signal to baseband signal directly, are suitable for small sized terminals used in land and satellite mobile communications [1]-[3]. An even harmonic mixing technique with anti-parallel diode pair (APDP) was proposed in [4], and a direct conversion receiver using it was proposed in [5]. This technique can reduce second order mixing products and LO noise[6]. But there are not many presentations about miniaturized even harmonic mixer circuits that are suitable for L- or S-band MMIC fabrications. Furthermore high isolation characteristics between in-phase(I) and quadrature-phase(Q) mixers is required to achieve low amplitude and phase error for a quadrature modulation and detection[7].

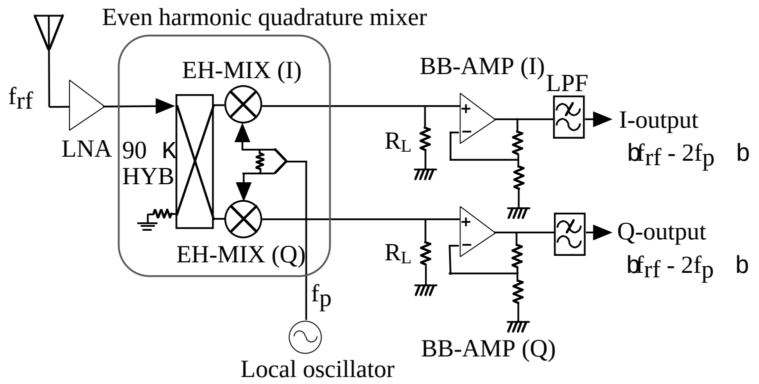
@ This paper presents a novel even harmonic quadrature ring mixer with an active matched 90 degree power divider and a ring connected APDP (RAPDP). A high isolation between the LO and RF ports can be achieved by the RAPDP in wide-band by applying the ring mixer concept to the even harmonic mixer. A novel active matched 90 degree power divider is proposed for suppressing amplitude and phase error over LO power variation. For fully monolithic integration on a GaAs substrate, this proposed circuit topology employs common gate FET (CGF) and common drain FET (CDF) that can be matched with the RAPDP and a phase shifter without any large sized circuit elements. Furthermore, a 2GHz band monolithic even harmonic quadrature ring mixer with an active balun was developed to confirm the effectiveness of the proposed configuration.

Configuration

Figure 1 shows a configuration of the direct conversion receiver with an even harmonic quadrature mixer[6]. This mixer consists of two even harmonic mixers, 90 degree power divider for RF signal (f_{rf}) and in-phase power divider for LO (f_p). RF signal and a second harmonic component of LO are mixed by the even harmonic quadrature mixer. Baseband output signal ($|f_{rf}-2f_p|$) produced at load resistance R_L, is amplified by baseband circuits including amplifiers and filters for channel selection. This circuit configuration with the even harmonic quadrature mixer has advantages that second order distortion and LO noise are low[6].

Figure 2 indicates a configuration of the proposed even harmonic quadrature ring mixer. The mixer consists of an active loaded 90 degree power divider for RF signal and even harmonic ring mixers for I- and Q-detections. A RAPDP is employed to achieve wide-band isolation characteristic. Also, to reduce chip-size, the proposed mixer employs lumped-elements for 90 degree phase shifting and active elements for combiner and divider circuits. The RF signal is divided equally into two RAPDPs by an active loaded 90 degree power divider. Then $|f_{rf}-2f_p|$ is output to BB port. An output load R_L is designed to be high impedance to achieve higher voltage conversion gain[6].

Figure 3 indicates a configuration of the active matched 90



90 KHYB : 90 degree hybrid power divider
EH-MIX : Even harmonic mixer
BB-AMP : Baseband amplifier
LNA : Low Noise Amplifier
LPF : Low Pass Filter

Fig.1. A configuration of even harmonic direct conversion receiver with an even harmonic mixer.

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degree power divider. This power divider consists of an active power divider with CDFs, HPF/LPF type phase shifter and CGFs. This proposed power divider has three technical features to achieve low error characteristics of quadrature detections as follows:

(a) Active power division by CDF can achieve high isolation characteristics for suppressing interferences between I- and Q- mixers, because the isolation between gate/source of CDF is quite high in low frequency region like L- or S-band.

(b) Active load by CGF can suppress RAPDP's impedance Zr variations due to LO level variations, and can provide impedance matching between the phase shifter and RAPDP. The RAPDP is connected with output port of the phase shifter. So stable load impedance is important for the phase shifter to attain low error characteristics.

(c) Trans-impedance function of CDF and CGF can suppress reflections without any large sized matching circuits. It is an effective technique for a small sized chip.

Figure 4 indicates an configuration of the even harmonic

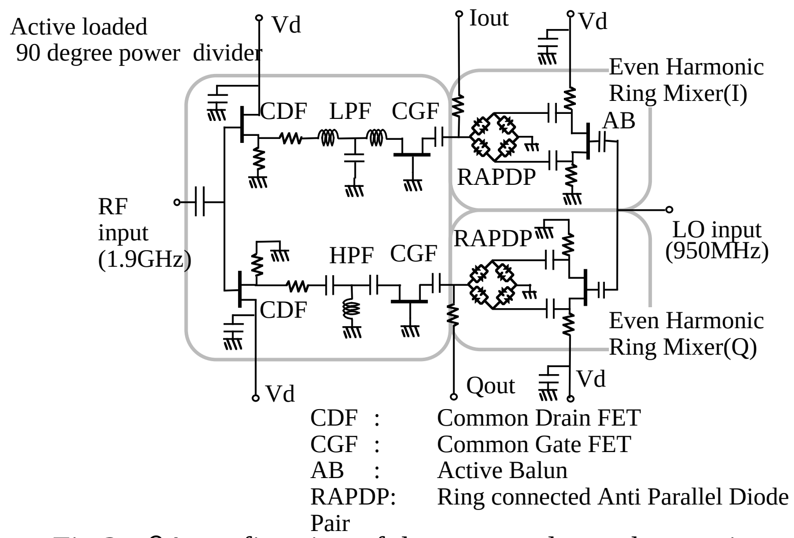

Fig.2. @A configration of the proposed even harmonic quadrature ring mixer.

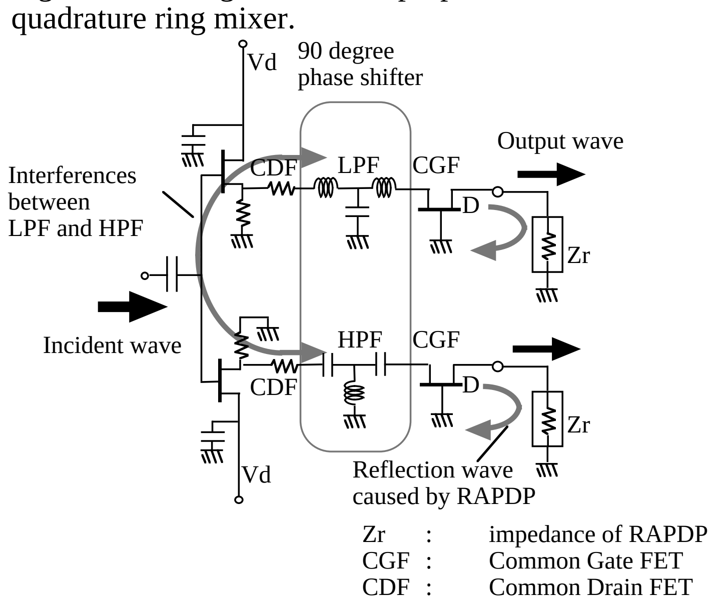

Fig.3. A configration of the proposed active matched 90 degree power divider. This circuit employs CGFs and CDFs to reduce amplitude and phase error degradation caused by LO variations of RAPDP.

ring mixer with an active balun. This mixer consists of an active balun for 180 degree power division and RAPDP. An isolation between the LO port and RF port can be obtained in wide-band by applying a ring mixer concept to the even harmonic mixer. The active balun supplies LO in 180 degree phase difference to RAPDP, then electric field of LO, E_{lo}, is fed as shown in Figure 3. This E_{lo} is canceled at the RF port, thus it is not output to RF port. In the same manner, RF is not output to LO port. A base-band output signal $|f_{rf}-2f_{p}|$ indicated as electric field E_{bb} is output to BB port.

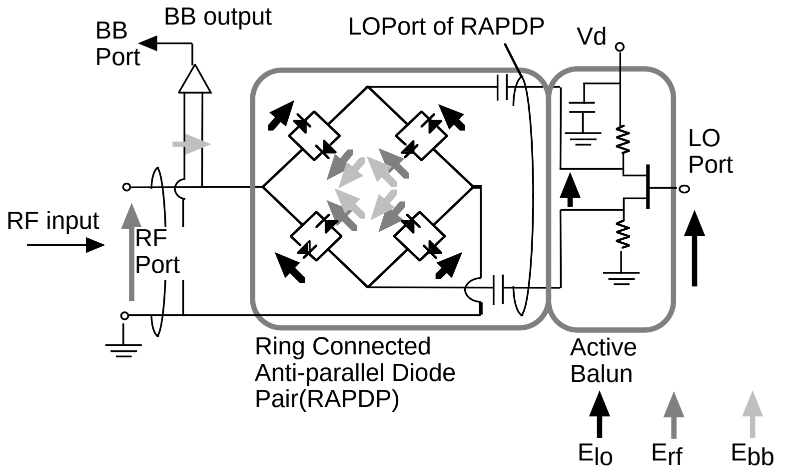

Fig.4. @A configration of the even harmonic ring mixer with an active balun.

Design of 2GHz mixer

In this section, design results are presented. They indicate the effectiveness of the proposed configurations. In this design, SAG(Self-Aligned Gate) FETs[8][9] are employed to realize a low cost fabrication of MMIC.

Figure 5 indicates calculated return loss at output ports and isolation characteristics of the power divider with common drain FETs(CDFs) used in the proposed active matched 90 degree power divider. The return loss is more than 20dB for a 1.6 to 2.4GHz frequency range. Also the isolation is more than 25dB for the 1.6 to 2.4GHz range. Thus the contribution of phase error [7] can be expected to be negligibly small.

Figure 6(a) indicates the return loss of RAPDP observed from the phase shifter. Figure 6(b) indicates amplitude error and phase error of the proposed active matched 90 degree power divider. These charts indicate characteristics versus RAPDP's impedance Zr and demonstrate effectiveness of CGF. Amplitude and phase errors do not varied since the amount of reflection remains constant when CGF is employed. Stable quadrature detection versus LO power variation can be achieved by the proposed active matched 90 degree power divider.

The isolation characteristic of ring mixer between LO and RF ports is degraded by unbalanced components in a balun, in general. The isolation Is of ring mixer with an active balun can be formulated as follows:

$$Is = \frac{1}{2}\sqrt{1-2\alpha\cos\Delta\theta+\alpha^2}\cdot\frac{\sqrt{A^2+B^2}}{\sqrt{C^2+D^2}}$$ @ @ @ @ @

$$\alpha = \frac{A}{\sqrt{A^2+B^2}},\quad \Delta\theta = \tan^{-1}\frac{-D}{C} - \tan^{-1}\frac{BC+AD}{-AC+BD}+\pi$$

$$A = k\cdot g_m,\ B=-\omega C_{gs}g_m,\ C=kG_d+k(k+g_m+G_d),\ D=\omega C_{gs}(G_d+k) \qquad (1)$$

where ¿ is the amplitude error and ¢ ˘is the phase error of an active balun, *k* is a constant related with a load resistance, ω is angular frequency, Cgs is gate to source capacitance and gm is trans-conductance. The complete isolation can be obtained in the case of Cgs=0. So in view of high isolation characteristics, FET with narrow gate width is suitable for the active balun. Also narrower FET requires low power consumption. But narrower FET has lower voltage gain. Thus gate width of FET has to be decided as a trade-off among isolation, voltage gain and power consumption. Figure 7 indicates calculated isolation, voltage gain and drain current of the active balun versus gate-width by harmonic balance method. As shown in the figure, isolation is high enough in such frequency region. The designing of the mixer needs to consider these 3 parameters. Here, the gate-width is set to 100 °m.

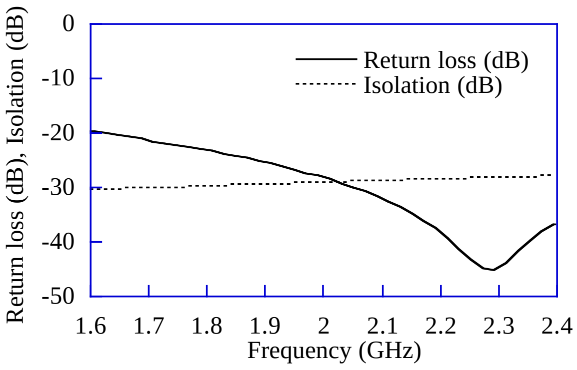

Fig.5. Calculated return loss at output ports and isolation characteristics of a proposed active power divider with common drain FETs(CDFs).

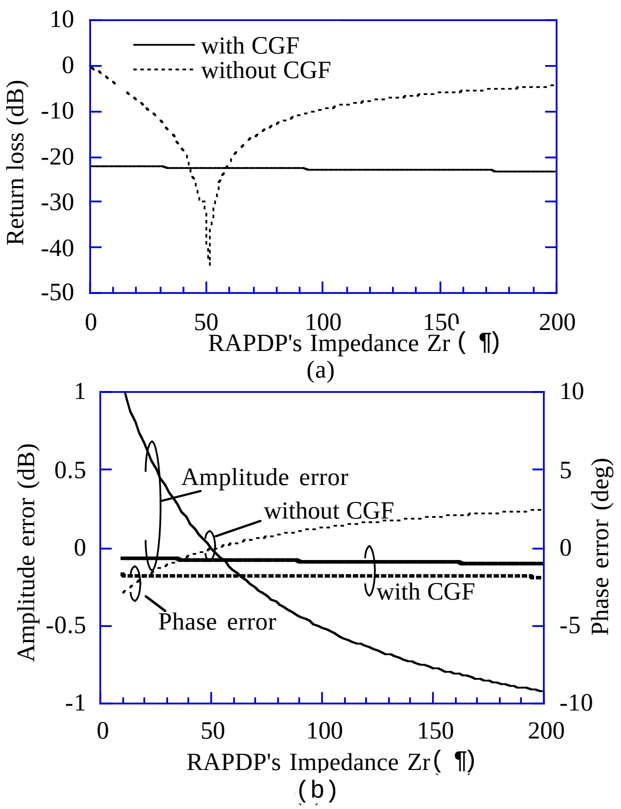

Fig.6 (a)The return loss of RAPDP observed from the phase shifter (b)Amplitude error and phase error of the proposed active matched 90 degree power divider.

Conversion Loss (dB)

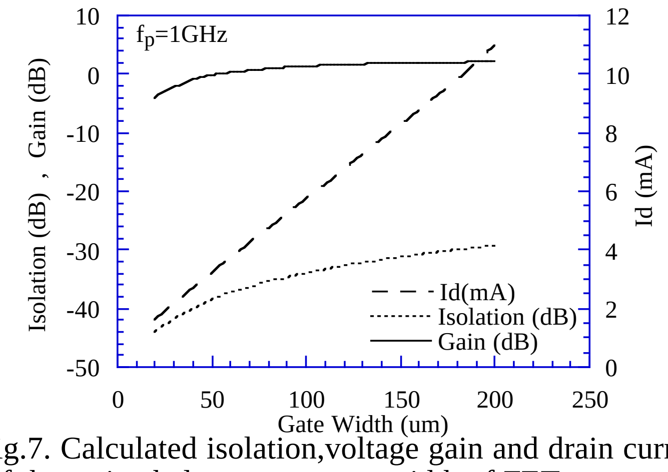

Fig.7. Calculated isolation,voltage gain and drain current of the active balun versus gate-width of FET. The results are calculated by harmonic balance method.

Experimental results of 2GHz mixer

Figure 8 indicates a photograph of the developed 2GHz monolithic even harmonic quadrature ring mixer. The size of the chip is 1.3mm ~1.85mm including all components of the quadrature detection by employing active matching circuits. The thickness of the substrate is 0.35mm to reduce phase error caused by capacitance between the patterns and a ground plane. SAG FETs [9] are employed for FET and APDP in the MMIC. Drain voltage of the circuits is 5V and drain current is 38mA.

Figure 9 indicates the voltage conversion loss of the monolithic even harmonic ring mixer. The conversion loss is below 10dB, including dividing loss of active matched 90 degree power divider. Figure 10 indicates amplitude and phase errors of the monolithic even harmonic quadrature ring mixer. The amplitude error is within }0.5dB and phase error is within }5 degrees for 1.7 to 2.3GHz frequency range. Figure 11 indicates the conversion loss, amplitude error and phase error versus LO power of the monolithic even harmonic quadrature ring mixer. The conversion loss is 8.5 ‘12.7dB, amplitude error

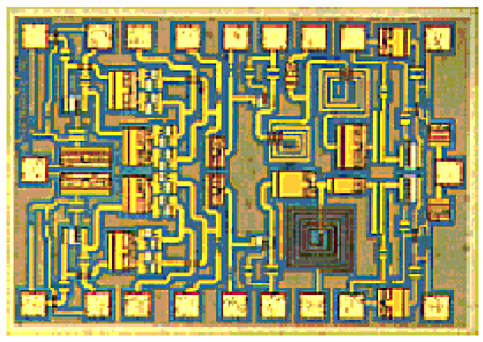

Fig.8. A photograph of the developed 2GHz monolithic even harmonic quadrature ring mixer.
The chip size is 1.8 ~1.3 ~ 0.35 mm^3 including two even harmonic quadrature mixers and 90degree power divider.

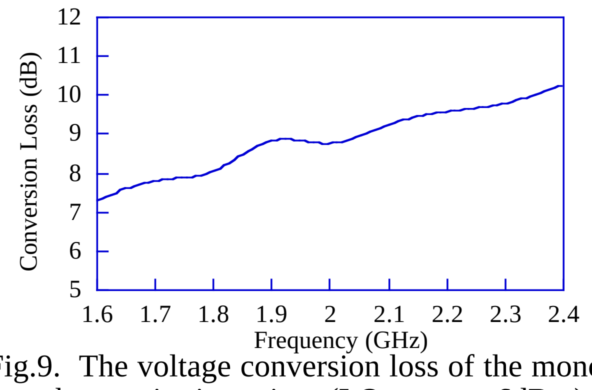

Fig.9. The voltage conversion loss of the monolithic even harmonic ring mixer (LO power : 6dBm).

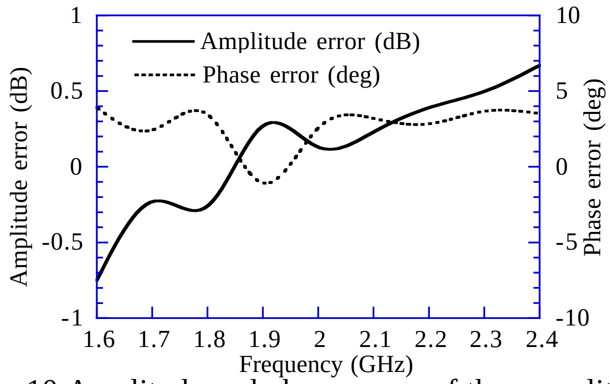

Fig.10 Amplitude and phase errors of the monolithic even harmonic ring mixer (LO power : 6dBm).

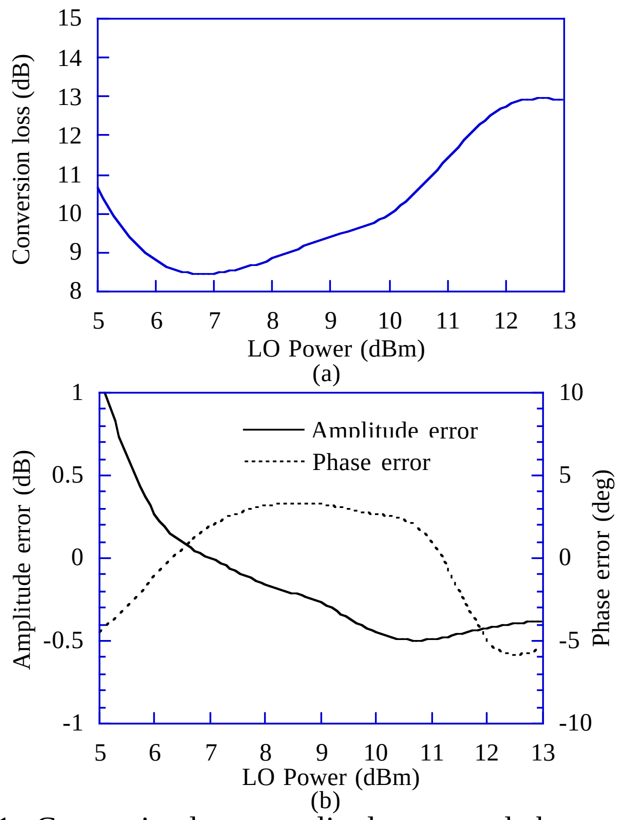

Fig.11. Conversion loss , amplitude error and phase error versus LO power of the monolithic even harmonic quadrature ring mixer.

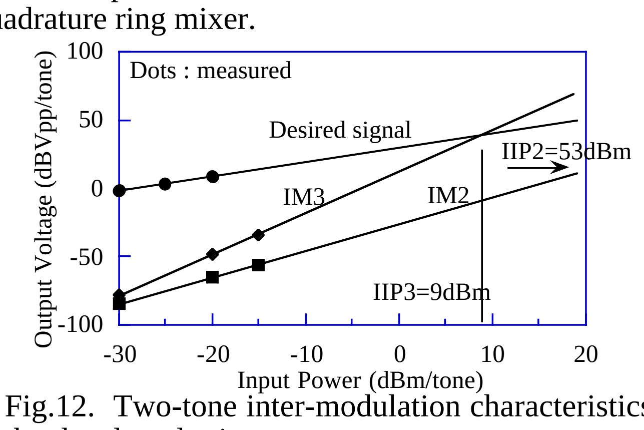

Fig.12. Two-tone inter-modulation characteristics of the developed mixer.

is within }0.5dB, and phase error is within }5 degrees for LO power range of 6 to 12dBm. The CGF gives stabilized quadrature accuracy over the variation of LO level.

Figure 12 indicates two-tone inter-modulation characteristics of the developed mixer. The intercept point of the second order inter-modulation (IIP2) at the input port is 53dBm and the intercept point of the third order inter-modulation (IIP3) at the input port is 9dBm, respectively. The high IIP2 can be achieved by employing the even harmonic mixing concept[6].

Measurement results shown above indicate that the developed mixer has excellent amplitude and phase error characteristics as the direct conversion receiver.

CONCLUSION

In this paper, a configuration of the even harmonic quadrature ring mixer was proposed. The developed MMIC contains all circuit elements for the quadrature detection and is small in size with 1.3mm ~1.85mm. The mixer achieved excellent characteristics for the wide-band reception by employing a ring mixer concept. Also, the stable characteristics with the variation of LO power can be achieved by the proposed active matched 90 degree power divider. Calculated and measured results indicate the effectiveness of the proposed configuration.

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